What is claimed is:

[Claim 1] 1. A clock circuit for generating an output clock in a data path according to a reference clock, in which there are signals of a plurality of periods, and each period of the signals has one rising edge and one falling edge, the clock circuit comprising:

a first flip-flop having a first clock port, wherein the first flip-flop generates a first signal according to triggering of a reference clock on the first clock port, and the first flip-flop changes a level of the first signal when each rising edge of reference clock occurs;

a second flip-flop having a second clock port, wherein the second flip-flop generates a second signal according to triggering of the reference clock on the second clock port, and the second flip-flop changes a level of the second signal when each falling edge of reference clock occurs; and

a logic module for performing a logic operation on the first signal and the second signal to generate the output clock.

[Claim 2] 2. The clock circuit in claim 1, wherein when the first flip-flop changes the level of the first signal at each rising edge of the reference clock, if the level of the first signal before the rising edge is a first level, the first flip-flop will change the level of the first signal to a second level after the rising edge.

[Claim 3] 3. The clock circuit in claim 2, wherein if the level of the first signal before the rising edge is the second level, the first flip-flop will change the level of the first signal to the first level after the rising edge.

[Claim 4] 4. The clock circuit in claim 1, wherein when the second flip-flop changes the level of the second signal at each falling edge of the reference clock, if the level of the second signal before the falling edge is a first level,

the second flip-flop will change the level of the second signal to a second level after the falling edge.

[Claim 5] 5. The clock circuit in claim 4, wherein if the level of the second signal before the falling edge is the second level, the second flip-flop will change the level of the second signal to the first level after the falling edge.

[Claim 6] 6. The clock circuit in claim 1, wherein the logic module comprises an XOR gate for generating the output clock according to results of an XOR operation between the first signal and the second signal.

[Claim 7] 7. The clock circuit in claim 1, wherein the clock circuit comprises a plurality of output pads to output signals of the clock circuit, and the reference clock is not output from any output pad.

[Claim 8] 8. A signal circuit, comprising:

a first circuit module for generating an output signal according to an input signal; the first circuit module comprising:
a first flip-flop having a first clock port, wherein the first flip-flop generates a first signal according to triggering of a reference clock on the first clock port, the reference clock comprising signals of a plurality of periods, each period of the signals having one rising edge and one falling edge, and the first flip-flop changes a level of the first signal when each rising edge of reference clock occurs;
a second flip-flop having a second clock port, wherein the second flip-flop generates a second signal according to triggering of the reference clock on the second clock port, and the second flip-flop changes a level of the second signal when each falling edge of reference clock occurs;
a first logic module for performing a logic operation on the first signal and the second signal to generate an output clock; and

a second logic module for performing a logic operation on the input signal and the output clock to generate the output signal.

[Claim 9] 9. The signal circuit in claim 8, wherein the input signal comprises a plurality of data and each data corresponds to one period of the reference clock.

[Claim 10] 10. The signal circuit in claim 8, wherein the second logic module performs an AND operation with the input signal and the output clock.

[Claim 11] 11. The signal circuit in claim 8, wherein when the first logic module generates the output clock, the output clock comprises a plurality of periods and each period of the output clock corresponds to one period of the reference clock so that the output clock is synchronous with the reference clock.

[Claim 12] 12. The signal circuit in claim 11, wherein to make each period of output clock correspond to one period of the reference clock, the level of the output clock in each period maintains a predetermined level during a predetermined time and the predetermined time is not longer than one period of the output clock.

[Claim 13] 13. The signal circuit in claim 12, wherein the input signal comprises a plurality of input data corresponding to one period of the reference clock, and that the second logic module performs the logic operation to make the output signal have a plurality of output data, wherein each output data corresponds to one period of the output clock.

[Claim 14] 14. The signal circuit in claim 13, wherein each output data has a first output sub-data and a second output sub-data, and each content of the

first output sub-data corresponds to one of the input data, and a continuation time of each second output sub-data corresponds to the predetermined time in one period of the output clock.

[Claim 15] 15. The signal circuit in claim 14, comprising:

a second circuit module for receiving the output signal according to triggering of a second reference clock;
wherein the second reference clock comprises a plurality of periods, and when the second logic module makes each first output sub-data correspond to one of the input data, the continuation time of the first output sub-data corresponds to one period of the second reference clock.

[Claim 16] 16. The signal circuit in claim 15, wherein when the second logic module makes each second output sub-data correspond to the predetermined time in one period of the input data, the continuation time of the second output sub-data corresponds to at least one period time of the second reference clock.

[Claim 17] 17. A method of generating an output clock in a data path according to a reference clock, the method comprising:

generating a first signal according to triggering of a reference clock so as to change a level of the first signal at each rising edge of the reference clock;
generating a second signal according to triggering of the reference clock so as to change a level of the second signal at each falling edge of the reference clock; and
performing a logic operation on the first signal and the second signal to generate the output clock.

[Claim 18] 18. The method in claim 17, wherein when the level of the first signal is changed at each rising edge of the reference clock, if the level of the

first signal before the rising edge is the first level, the level of the first signal is changed to the second level after the rising edge.

[Claim 19] 19. The method in claim 18, wherein if the level of the first signal before the rising edge is the second level, the level of the first signal is changed to the first level after the rising edge.

[Claim 20] 20. The method in claim 17, wherein when the level of the second signal is changed at each falling edge of the reference clock, if the level of the second signal before the falling edge is the first level, the level of the second signal is changed to the second level after the falling edge.

[Claim 21] 21. The method in claim 20, wherein if the level of the second signal before the rising edge is the second level, the level of the second signal is changed to the first level after the rising edge.

[Claim 22] 22. The method in claim 17, wherein when the first signal undergoes the logic operation with the second signal to generate the output clock, the first signal and the second signal undergo an XOR operation to generate the output clock.

[Claim 23] 23. The method in claim 17 further comprising generating a reference signal by using a ratio between the period of the first signal and that of the second signal before generating the output clock so that a duty cycle of the reference signal is different from that of the output clock.